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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,113	02/04/2004	Baker David	8479-059-999	3950

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EXAMINER	
JACOB, MARY C	
ART UNIT	PAPER NUMBER
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,113	DAVID, BAKER	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 have been presented for examination.

Specification

2. The disclosure is objected to because of the following informalities. Appropriate correction is required.

3. The disclosure does not contain headings such as those listed below.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a

> nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

4. Claims 5 and 7 are objected to because of the following informalities. Appropriate correction is required.

5. Claims 5 and 7 recite "a PLI routine is linked with a simulator and a control program is then used...". Although this claim language is interpreted to read, "a PLI routine is linked with a simulator, and a control program is then used...", the language should be clarified so that it is understood whether the PLI routine is linked with just the simulator or is linked with the simulator *and* the control program, and further, whether the control program alone is "used to force a test netlist...".

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claims 1 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: "automatically" testing the design.

The claims are directed to a method and apparatus to "automatically and statically" test a circuit design. However, they recite limitations for simulating the circuit, examining faults and modifying the circuit design. Although the limitations appear to be directed to testing a circuit design, it is unclear how this testing is done "automatically". It appears that a user can perform these steps, so that they are not necessarily "automatically" done.

9. Claims 1 and 6 further recite "modifying the circuit design...so that when the modified circuit design is retested...each flip-flop will not go metastable when the reset state is released, a stable state being achieved...when its output value does not change on a subsequent active clock transition". This language appears to be directed to defining how the circuit design is modified. Therefore, it is unclear if the modified design is actually "retested".

10. Claims 1 and 6 recite the limitation "the flip flop" in the limitation reciting "modifying the circuit design...". There is insufficient antecedent basis for this limitation in the claim. It is unclear whether the steps of modifying the circuit design are applied to just one flip-flop, or all the flip-flops in the design that need modification.

Claim Interpretation

11. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162

USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process.

12. Claims 1 and 6 recite reference characters in parenthesis. Section 608.01 (I) of the MPEP states: "Reference characters corresponding to elements recited in the detailed description and the drawings may be used in conjunction with the recitation of the same element or group of elements in the claims. The reference characters, however, should be enclosed within parentheses so as to avoid confusion with other numbers or characters which may appear in the claims. The use of reference characters is to be considered as having no effect on the scope of the claims." Therefore, the reference characters in Claims 1 and 6 are interpreted as having no effect on the scope of the claims.

Claim Rejections - 35 USC § 101

13. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

14. Claims 1-7 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1-7 are directed to a method and apparatus for "automatically and statistically testing the design of a simulated integrated circuit". This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring phenomenon) since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having a real world value rather than a result that may be interpreted to be abstract in nature, as, for example, a thought, a computation or manipulated data. More specifically, the claimed subject matter provides for "simulating a circuit", "listing the flip-flops" and "modifying the circuit design". These produced "results" remain in the abstract and thus, fails to achieve the required status of having a real world value. For example, there is no output of the testing results to a user or the storage of testing results that can be put to use in some practical application.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1, 5, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pomeranz et al ("On the Detection of Reset Faults in Synchronous Sequential

Circuits", 10th International Conference on VLSI Design, January 4-7. 1997, pages 470-474).

17. As to Claims 1 and 6, Pomeranz et al teaches: a method of automatically and statically testing the design of a circuit includes the steps of: simulating a circuit having a level containing a network of flip-flops (Configurations 1 and 2; Abstract, lines 2-4, 7-10; Procedures 1-5); putting the network in a reset state, in which each flip-flop would have an expected input and output state (Introduction, paragraph 3, lines 7-10; Procedure 1, steps 1 and 2; Procedure 2, steps 1 and 2); scanning the network to obtain the input and output states (Procedure 1, steps 3-5; Procedure 2, steps 3-5; Section 2, paragraph 4, lines 3-6); detecting the flip-flops with other than the expected input and output states as having potential faults (section 3, paragraph 4, "A fault $f_{i,1}$ is detected..."); examining each potential fault; and modifying the circuit design so as to change the reset state of the flip-flop so that when the modified design is retested by putting the network into a reset state and by releasing the reset state, each flip-flop will not go metastable when the reset state is released, a stable state being achieved in said flip-flop when its output value does not change on a subsequent active clock transition (section 3, paragraph 1, lines 1-5, paragraph 2, lines 1-3; Procedure 3, step 2(a), paragraph 5, lines 7-15, paragraph 6, lines 1-3; Procedure 3, step 2).

18. As to Claims 5 and 7, Pomeranz et al teaches: wherein a PLI routine is linked with a simulator and a control program is then used to force a test netlist into a reset state (Introduction, paragraph 3, lines 7-10; Procedure 1, steps 1 and 2; Procedure 2, steps 1 and 2); a PLI code being called to detect the state of the inputs and outputs of

each flip-flop and faults that are detected for a flip-flop (Procedure 1, steps 3-5; Procedure 2, steps 3-5; Section 2, paragraph 4, lines 3-6; section 3, paragraph 4, "A fault $f_{i,1}$ is detected...") and post-processing the information to show the number and type of fault detected in each circuit, each circuit being a network of flip-flops (Table 1 and description).

19. Pomeranz et al does not expressly teach: (claims 1 and 6) listing flip-flops with other than the expected input and output states; (claims 5 and 7) the logging of the states of inputs and outputs, the logged information being post-processed to create a list of flip-flops that have potential faults.

20. Pomeranz et al teaches obtaining the input and output states (Procedure 1, steps 3-5; Procedure 2, steps 3-5; Section 2, paragraph 4, lines 3-6), the detection of flip-flops with faults (section 3, paragraph 4, "A fault $f_{i,1}$ is detected...") and further, the treatment of these flip flops with faults (Procedure 3 and description). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the detection of these input and output states as well as the detection of flip-flips with faults would require the and "logging" or "listing" of these input/output states and of the flip flops that have faults somewhere in a storage element of a computer in order set values of P_{ff} and Z_{ff} to the next-state and output values (as discussed in Procedure 1, steps 4-5, for example) and to further treat the faulty flip flops in the circuit being tested as (discussed in Procedure 3) and to list the total amounts of faults occurring in a circuit made up of flip-flops (Table 1 and description).

21. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pomeranz et al as applied to claim 1 above, in view of Nelson et al ("Digital Logic Circuit Analysis and Design", Prentice Hall, 1995, Section 6.4).

22. Pomeranz et al teaches automatically and statically testing the design of a circuit containing a network of flip-flops.

23. Pomeranz et al does not expressly teach: (claim 2) wherein the flip-flops are of the D Type; (claim 3) wherein the flip-flops are of the T type; (claim 4) wherein the flip-flops are of the J-K type.

24. Nelson et al teaches D, T and J-K flip-flops are types of flip-flops known in the art (section 6.4.2; section 6.4.3; section 6.4.6).

25. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the automatically and statically testing the design of a circuit containing a network of flip-flops as taught in Pomeranz et al to include the flip-flops as tested in Pomeranz et al being of a D, T or J-K type since Nelson et al shows that D, T and J-K flip-flops are common types of flip-flops known in the art.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

27. International Search Report for PCT/GB98/03384.

28. Liang et al ("Identifying Invalid Test States for Sequential Circuit Test Generation", IEEE Transactions on Computer-Aided Design of Integrated Circuits and

Systems, Col. 16, No. 9, September 1997) teaches algorithms to identify, before test generation, invalid states for sequential circuits without reset states.

29. Glaser et al ("Mixed Level Test Generation for Synchronous Sequential Circuits Using the FOGBUSTER Algorithm", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, No. 4, April 1996) teaches test generation for synchronous sequential circuits that implements two levels of hierarchy, the switch level and the gate-level.

30. Gonzalez et al (WO 94/23388) teaches evaluating the output state of a flip-flop, indicating asynchronism, and reassigning the output states based on this indication.

31. Trimberger (US Patent 5,650,946) teaches an event-driven simulation wherein the system allows the user to access the simulation history during the simulation, make changes to the state of the circuit at any time recorded within the simulation history, and resume the simulation of the circuit automatically corrected for any changes.

32. Glunz et al (US Patent 5,502,661) teaches a method for checking conformance of a digital circuit design, wherein stimuli is simulated through a circuit description until a stable state is reached, and then the simulation model is switched into check mode in which each component of the circuit checks a testability state and issues error messages if an illegal state was found.

33. Patents recited in parent case, US Application 09/529126: 5,345,393; 5,550,839; 5,838,693; 5,584,020.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Mary C. Jacob
Examiner
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3/26/07

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